REMARKS

Claims 1, 11 and 14 have been amended. No claims have been added or canceled. Accordingly, claims 1-15 are currently pending in the application.

PRIORITY

Submitted herewith is a certified copy of the priority document, JP 2001-125219, filed April 24, 2001. Acknowledgement of the claim for priority under 35 U.S.C. 119 and an indication that this document has been safely received would be appreciated.

DRAWINGS

Approval is hereby requested for a proposed drawing correction to Figures 2-4 in order to label them prior art. Replacement sheets of formal drawings are attached.

35 U.S.C. § 102(b) and 103(a)

Claims 1-4 and 10-15 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,814,529 (Zhang). Claims 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,814,529 (Zhang) in view of U.S. Patent No. 6,317,173 (Jung). Claim 6 is rejected under

35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,814,529 (Zhang) in view of U.S. Patent No. 5,998,838 (Tanabe). Finally, claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,814,829 (Zhang) in view of U.S. Patent No. 6,046,790 (Hara). These rejections are traversed as follows.

According to the present invention, as defined by claims 1 and 14, a second insulation film is provided only on the upper surfaces and side surfaces of a gate electrode and a storage electrode. Therefore, this second insulation film does not exist on the periphery of contact holes. As a result, the contact holes can be formed using a single mask. In addition, since the second insulation film does not exist at the pixel portion (i.e., the back light transparent area) higher contrast can be obtained.

On the other hand, Zhang uses two masks in order to form contact holes 113 and 114. The diameter of the contact holes 113, 114 should be smaller than that of openings 110, 111 (see column 3, lines 48-50). Therefore, the diameter of the openings 110, 111 must become larger in order to take into consideration errors in positioning of the masks. Therefore, the degree of integration of the circuit is reduced. Furthermore, Zhang's second insulation film 108 is formed all

over the substrate, thereby lowering transparency of the back light and lowering contrast.

Furthermore, according to Zhang's second embodiment, contact holes 214, 215 are formed using pixel electrode 213 or a mask as a second mask. This method is similar to that discussed in the background of the present specification on pages 4 and 5 (see discussion of JP-A-11-271812). This method causes problems in that the thickness of the insulating film forming the capacitor becomes uneven due to an ITO (indium tin oxide) etchant. A reactant layer of the ITO and the insulation film is formed which thereby decreases storage capacitance.

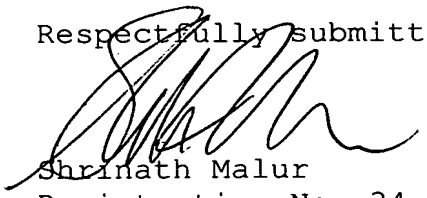
According to present claim 11, an interlayer insulation film is formed and then contact holes are formed. Thereafter, the second insulation film is formed. This is done to avoid any damage to the second insulation layer when the interlayer insulation film 10 is etched.

On the other hand, according to Zhang, the interlayer insulation film is formed and etched after all of the second insulation film is formed. As such, Zhang's method cannot realize the advantages of the present invention.

CONCLUSION

In view of the foregoing amendments and remarks the Applicants contend that the above-identified application is now in condition for allowance. Accordingly, reconsideration is hereby requested.

Respectfully submitted,



Shrinath Malur
Registration No. 34,663
Attorney for Applicant(s)

MATTINGLY, STANGER & MALUR, P.C.
1800 Diagonal Road, Suite 370
Alexandria, Virginia 22314
Telephone: (703) 684-1120
Facsimile: (703) 684-1157
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